

1079

5100 U.S. 879 PRO  
5109/825279

		Subclass
	Class	

**PATENT NUMBER**

**U.S. UTILITY Patent Application**

<b>I.P.E.</b>	<b>PATENT DATE</b>
<i>John G. Kelly</i> SCANNED <i>John G. Kelly</i> Q.A. <i>John G. Kelly</i>	

APPLICATION NO. 09/825279	CONT/PRIOR F	CLASS 324	SUBCLASS 111	ART UNIT 2858	EXAMINER M. O. I. C. Dee
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Marcus Kuegler  
Ali Badiei

## Method and apparatus for testing digital circuitry

TIME

PTD-2040  
12/99

## **ISSUING CLASSIFICATION**

<input type="checkbox"/> TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	(Assistant Examiner)			<b>NOTICE OF ALLOWANCE MAILED</b>	
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____ _____ _____	(Primary Examiner)				
<input type="checkbox"/> The terminal ____ months of this patent have been disclaimed.	(Legal Instruments Examiner)			<b>ISSUE FEE</b>	
				<b>ISSUE BATCH NUMBER</b>	

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